

Features

- Operating voltage: 2.4V~12V
- Low power and high noise immunity CMOS technology
- Low stand-by current
- Capable of decoding 12 bits of information
- Pairs with HOLTEK's 2¹² series of encoders
- Binary address setting
- Three times of receiving check

Applications

- Burglar alarm system
- Smoke and fire alarm system
- Garage door controllers
- Car door controllers

General Description

The 2^{12} decoders are a series of CMOS LSIs for remote control system applications. They are paired with HOLTEK's 2^{12} series of encoders (refer to the encoder/decoder cross reference table). For proper operation a pair of encoder/decoder with the same number of addresses and data format should be chosen.

The decoders receive serial addresses and data from a programmed 2^{12} series of encoders that are transmitted by a carrier using an RF or an IR transmission medium. They compare the serial input data three times continuously with

- Address/Data number combination:
 - HT12D: 8 address bits and 4 data bits
- HT12F: 12 address bits and 0 data bit
- A built-in oscillator with only a 5% resistor
- A valid transmission indicator
- Easy interface with an RF or an Infra-Red transmission medium
- Minimal external components
- Car alarm system
- Security system
- Cordless telephones
- Other remote control systems

their local addresses. If no error or unmatched codes have been found, the input data codes are decoded and then transferred to the output pins. The VT pin also goes high to indicate a valid transmission.

The 2¹² series of decoders is capable of decoding information that consists of N bits of address and 12–N bits of data. Of this series, the HT12D is arranged to provide 8 address bits and 4 data bits, and the HT12F is used to decode 12 bits of address information.

Selection Table

Function	Address	Address Data		VT	Oscillator	Tuisson	Package	
Item	No.	No.	Туре	VI	Uscillator	Trigger	Раскаде	
HT12D	8	4	L		RC oscillator	DIN active "Hi"	18 DIP/20 SOP	
HT12F	12	0		\checkmark	RC oscillator	DIN active "Hi"	18 DIP/20 SOP	

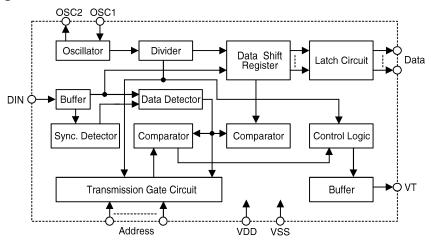
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Note: Data type — M represents the momentary type of data output — L represents the latch type of data output

VT can be used as a momentary data output



Block Diagram

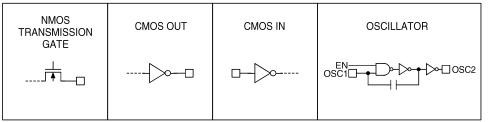


Note: The address/data pins are available in various combinations (see the address/data table).

Pin Description

Pin Name	I/O	Internal Connection	Description
A0~A11	Ι	NMOS TRANSMISSION GATE	Input pins for address A0~A11 setting They can be externally set to VDD or VSS.
D8~D11	0	CMOS OUT	Output data pins
DIN	Ι	CMOS IN	Serial data input pin
VT	0	CMOS OUT	Valid transmission, active high
OSC1	Ι	OSCILLATOR	Oscillator input pin
OSC2	0	OSCILLATOR	Oscillator output pin
VSS	Ι		Negative power supply (GND)
VDD	Ι		Positive power supply

Approximate internal connection circuits



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Absolute Maximum Ratings

Supply Voltage	0.3V to 13V
Input Voltage	. V_{SS} –0.3 to V_{DD} +0.3V

Storage Temperature50°C t	o 125°C
Operating Temperature20°C	to 75°C

Electrical Characteristics

6h - l	Demonster	Т	est Condition	M*	T			
Symbol	Parameter	VDD	Condition	Min.	Тур.	Max.	Unit	
VDD	Operating Voltage	_	_	2.4	5	12	V	
Lamp	Stand by Cumant	5V	Occillator store	_	0.1	1	μΑ	
ISTB	Stand-by Current		Oscillator stops.	_	2	4	μΑ	
I _{DD}	Operating Current	5V	No load F _{OSC} =150KHz		200	400	μΑ	
L	Data Output Source Current (D8~D11)	5V	V _{OH} =4.5V	-1	-1.6	_	mA	
Io	Data Output Sink Current (D8~D11)	5V	V _{OL} =0.5V	1	1.6	_	mA	
T	VT Output Source Current	5V	V _{OH} =4.5V	-1	-1.6	_	mA	
Ivt	VT Output Sink Current		Vol=0.5V	1	1.6	_	mA	
VIH	"H" Input Voltage	5V		3.5	_	5	V	
VIL	"L" Input Voltage	5V	_	0	_	1	V	
FOSC	Oscillator Frequency	5V	$R_{OSC}=51K\Omega$	_	150	_	KHz	

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Functional Description

Operation

The 2^{12} series of decoders provides various combinations of addresses and data pins in different packages so as to pair with the 2^{12} series of encoders.

The decoders receive data that are transmitted by an encoder and interpret the first N bits of code period as addresses and the last 12–N bits as data, where N is the address code number. A signal on the DIN pin activates the oscillator which in turn decodes the incoming address and data. The decoders will then check the received address three times continuously. If the received address codes all match the contents of the decoder's local address, the 12–N bits of data are decoded to activate the output pins and the VT pin is set high to indicate a valid transmission. This will last unless the address code is incorrect or no signal is received.

The output of the VT pin is high only when the transmission is valid. Otherwise it is always low.

Output type

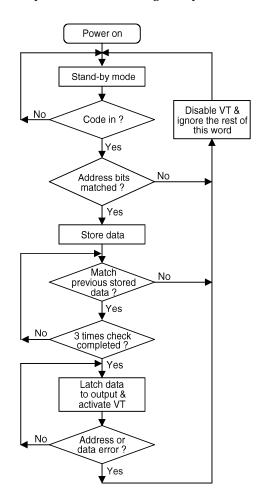
Of the 2^{12} series of decoders, the HT12F has no data output pin but its VT pin can be used as a momentary data output. The HT12D, on the other hand, provides 4 latch type data pins whose data remain unchanged until new data are received.

	Data Pins	ata Address Output ins Pins Type			
HT12D	4	8	Latch	2.4V~12V	
HT12F	0	12		2.4V~12V	

Flowchart

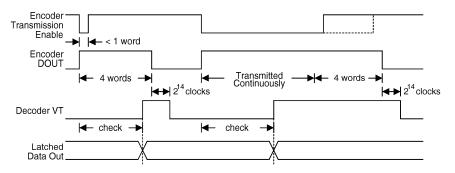
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The oscillator is disabled in the stand-by state and activated when a logic "high" signal applies to the DIN pin. That is to say, the DIN should be kept low if there is no signal input.





Decoder timing diagram



Encoder/Decoder cross reference table

					Package				
Decoders Part No.	Data Pins	Address Pins	VT	Pair Encoder	Encoder		Decoder		
					DIP	SOP	DIP	SOP	
HT12D	4	8	0	8 1	HT12A/B	18	20	18	20
ΠΙΙΔΟ	4		v	HT12E	18	20	10	۵0	
LIT19E	0	12		HT12A/B	18	20	18	20	
HT12F	0	12	N	HT12E	18	20	10		

Address/Data sequence

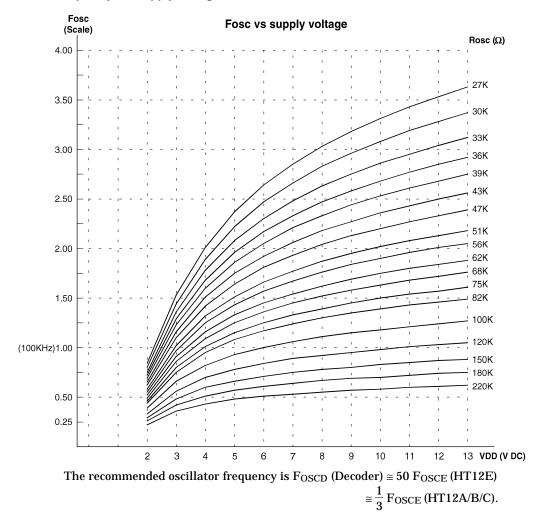
The following table provides a address/data sequence for various models of the 2^{12} series of decoders. A correct device should be chosen according to the requirements of individual addresses and data.

HOLTEK		Address/Data Bits										
Part No.	0	1	2	3	4	5	6	7	8	9	10	11
HT12D	A0	A1	A2	A3	A4	A5	A6	A7	D8	D9	D10	D11
HT12F	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11

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Oscillator frequency vs. supply voltage



15th Mar '96

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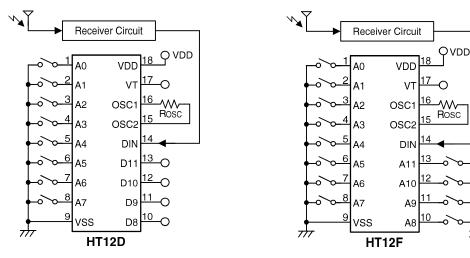
Package Information

8 Address 4 Data		8 Address 4 Data		12 Address 0 Data	•	12 Address 0 Data	
A0 🗆 1		NC 1 A0 2	20 DNC 19 DVDD		18 VDD	NC [] A0 2	20 NC 19 VDD
A1 □ 2 A2 □ 3	17□VT 16□OSC1	A1 🗖 3 A2 🗖 4	18□VT 17□OSC1	A1 🗆 2 A2 🗖 3	17□VT 16□OSC1	A1 □ 3 A2 □ 4	18 □ VT 17 □ OSC1
A3 🗆 4	15 0SC2	A3 🗆 5	16 05C2	A3 🗆 4	15 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	A3 🗆 5	16 🗆 0501
A4 🗖 5		A4 🔤 6	15 DIN	A4 🗖 5	14 DIN	A4 🔤 6	15 DIN
	13 D11		14 🗆 D11 13 🗆 D10		13 🗆 A11		
A6 🗖 7 A7 🗖 8	12 D10 11 D9	A6 □ 8 A7 □ 9		A6 🗆 7 A7 🗖 8	12 🗆 A10 11 🗖 A9	A6 □ 8 A7 □ 9	13 □ A10 12 □ A9
VSS 🗆 9	10 D8		11 D8	VSS 🗆 9	10 A8	VSS I 10	
HT1 - 18		HT1 - 20 \$		HT1 – 18		HT1 - 20 \$	

Application circuit 2

Application Circuits





Note: Typical infrared receiver: PIC-12043T/PIC-12043S (KODESHI CORP.) or LTM9052 (LITEON CORP.)

Typical RF receiver: JR-200 (JUWA CORP.) RE-99 (MING MICROSYSTEM, U.S.A.) FO-493RX (FISCHER-OLSEN, GERMANY)

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